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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,636	03/29/2001	Hiroyuki Ikeda	075834.00064	5712

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EXAMINER	
TRAN, THIEN F	
ART UNIT	**PAPER NUMBER**
2895	

MAIL DATE	DELIVERY MODE
09/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/821,636	IKEDA, HIROYUKI	
	Examiner	Art Unit	
	Thien F. Tran	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 39-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 39-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/20/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 07/20/2009 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 39-41are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai et al (US 5,644,146).

Regarding claims 1 and 39, Arai et al discloses a display apparatus (liquid crystal display, col. 1, lines 9-10) comprising a thin film transistor, the thin film transistor comprising a semiconductor thin film (21') constituting a channel (M portion) and having a threshold voltage (see Table 1), and a first gate electrode (front gate electrode 6) on one side of said semiconductor thin film and a second gate electrode (rear gate electrode 2) on an opposite side of said semiconductor thin film, and further comprising

a means (col. 4, lines 38-59) for adjusting the threshold voltage by applying a first threshold adjustment voltage (rear gate voltage -5V) to the second gate electrode (2) when the first gate electrode (6) receives a first control voltage (V_G, see Fig. 6) and applying a second threshold adjustment voltage (rear gate voltage -4V) different than the first threshold adjustment voltage to the second gate electrode (2) when the first electrode receives a second control voltage (V_G, see Fig. 6). Arai et al does not explicitly disclose that the liquid crystal display comprising a plurality of thin film transistors. However, it is a known fact that the conventional liquid crystal display comprises a plurality of thin film transistors. Therefore, forming the plurality of thin film transistors in the conventional liquid crystal display using the thin film transistor as taught by Arai et al would have been prima facie obvious to provide thin films transistors which has no avalanche effect and in which the threshold voltage is adjustable.

Regarding claim 2, the semiconductor thin film (21') constituting the channel is comprised of polycrystalline silicon. Arai et al. further discloses that the thin film transistor is a P-channel thin film transistor (col. 5, lines 23-25). It is well known that for P-channel transistors, the channel is doped of n-type impurity which is either phosphorus or arsenic. Therefore, the channel does not contain boron which is a p-type impurity that effectively affects the formation of a depletion layer. Arai does not disclose the semiconductor thin film (21') having a thickness of 100 nm or less. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the semiconductor thin film having the claimed range of thickness, since it has been held that where the general conditions of a claim are disclosed in the

prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 3, the semiconductor thin film (21') constituting the channel is comprised of polycrystalline silicon. Arai et al. further discloses that the thin film transistor is an N-channel thin film transistor (col. 4, lines 53-55). It is well known that for N-channel transistors, the channel is doped p-type impurity such as boron which inherently contains an impurity effectively affecting the formation of a depletion layer. Arai et al does not explicitly disclose the semiconductor thin film having a thickness two times or less the maximum of the thickness of the depletion layer. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the semiconductor thin film having the claimed range of thickness, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 40 and 41, Fig. 6 of Arai et al. discloses the voltage (V_G at 5V) applied to the first gate electrode (front gate electrode 6) is different from the threshold adjustment voltage (-5V for sample No. 1) applied to the second gate electrode (rear gate electrode 2) during voltage application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-

1665. The examiner can normally be reached on 7:30AM - 4:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thien F Tran
Primary Examiner
Art Unit 2895

/Thien F Tran/
Primary Examiner, Art Unit 2895